

CompE 470 – Digital Circuits

Summer 2004

Instructor Information:

Dr. Khurram Waheed.

Office: 202-B Engineering Building
Office Hours: Mon-Thurs. 2:00 pm – 3:00 pm (and by appointment)
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Class Schedule:

Time: Mon-Thurs. 12:00 pm – 1:45 pm
Classroom: E-423B
Website <http://attila.sdsu.edu/~waheed/compe470>

Course Objectives:

1. Understand how to design modern programmable logic devices such as PLDs, FPGAs and ASICs.
2. To obtain engineering knowledge on the theory and practices involved in the CAD based design of digital systems and their modeling, simulation, synthesis and testing.
3. Get familiar with all phases of digital system development, i.e., understand design flow from initial specification to testable synthesized circuits in a PLD/ FPGA/ASIC.
4. Learn the design and modeling of combinatorial and synchronous logic circuits, finite state machines, mathematical units, data/control paths and test harnesses using HDL (Hardware Design Languages) such as VHDL.
5. To learn a VHDL CAD tool (such as Xilinx Inc. ISE™) for simulation, synthesis and timing analysis of digital systems.
6. To evaluate design and timing performance using CAD tools.

Text:

- *Douglas J. Smith*; HDL Chip Design: A Practical Guide for Designing, Synthesizing, and Simulating ASICs and FPGAs using VHDL or Verilog; 6th Ed. ISBN 0-9651934-3-8, Doone Publications
- Additional class handouts and resources (if required will be made available via the class website)

References:

- *S. Yalamanchili*, Introductory VHDL from Simulation to Synthesis, Prentice-Hall, 2001.
- *Z. Navabi*, VHDL: Analysis and Modeling of Digital Systems, 2nd Ed., McGraw Hill, 1998.
- *M. D. Cilette*, Advanced Digital Design With Verilog HDL, Prentice-Hall 2002
- *P. J. Ashenden*, The Designer's Guide to VHDL, 2nd Ed., Morgan Kaufmann, 2001.
- *C. H. Roth*, Digital Systems Design Using VHDL, PWS, 1998.
- *Pellerin and Taylor*, VHDL Made Easy!, Prentice Hall, 1997.

- *Brown and Vranesic*, Fundamentals of Digital Logic with VHDL Design, McGraw-Hill, 2000.
- *J. F. Wakerly*; Digital Design: Principles and Practices 3rd Ed. Prentice Hall, 2001.

Prerequisites: CompE 270.

Topics Covered:

1. Introduction to CPLDs, FPGAs, CAD Tools, Physical Design Constraints: ¾ weeks
2. VHDL Language fundamentals: 1 ½ weeks
3. Modeling of combinational circuits & devices with VHDL: 1 weeks
4. Modeling of sequential systems and finite state machines using VHDL: 2 weeks
5. Writing VHDL for test harnesses and signal generation: ½ week
6. Incorporating Timing parameters, Tri-state buffers: ½ week
7. VHDL modeling, simulation and synthesis issues. 1 weeks
8. Structuring a VHDL design project: ½ week
9. Design and modeling of data and control path: ½ weeks.

Credit Distribution:

Homeworks/Projects	15 %	
Midterm 1	20 %	Monday June 7, 2004
Midterm 2	25 %	Tuesday June 22, 2004
Final Project	15 %	<i>Assigned:</i> June 14, 2004, Due June 30, 2004
Final Exam	25 %	Thursday July 1, 2004

Notes:

- The Final Project will be a comprehensive digital system design (typically involving FSM design and/or datapath controller) to be submitted as a professional style report with accompanying design data.
- A student who finds it necessary to miss an exam should contact the professor before the exam to explain the circumstances, according to SDSU policy. No make-up exams will be given.
- A student who misses the final exam without satisfactory explanation will receive a failing grade in the course according to SDSU policy.